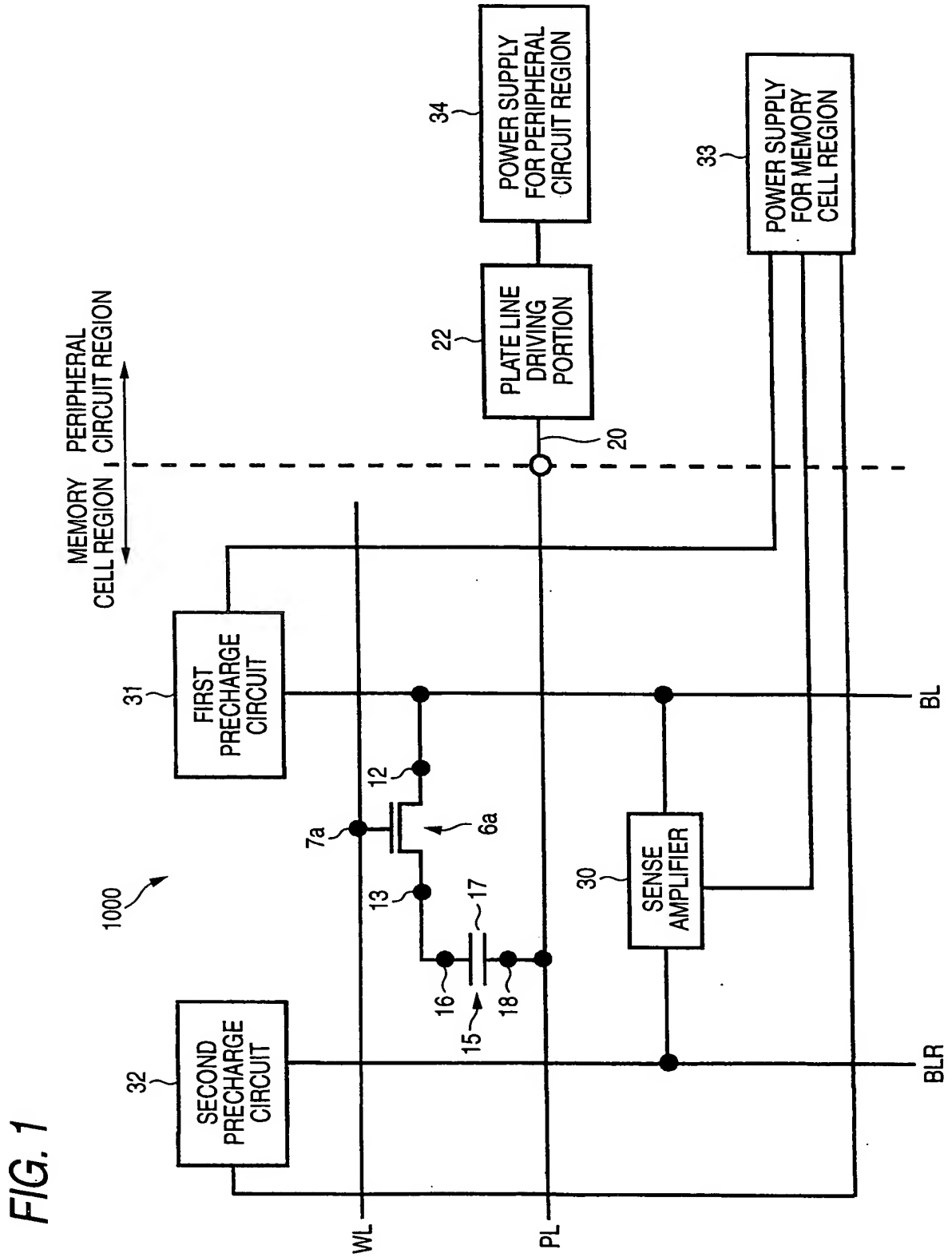

POWER SUPPLY FOR PERIPHERAL CIRCUIT REGION
34
POWER SUPPLY FOR MEMORY CELL REGION
33
PLATE LINE DRIVING PORTION
22
20
PERIPHERAL CIRCUIT REGION
MEMORY CELL REGION
FIRST PRECHARGE CIRCUIT
31
BL
12
7a
6a
1000
13
17
SENSE AMPLIFIER
30
16
18
15
SECOND PRECHARGE CIRCUIT
32
BLR
WL
PL

FIG. 1

FIG. 2

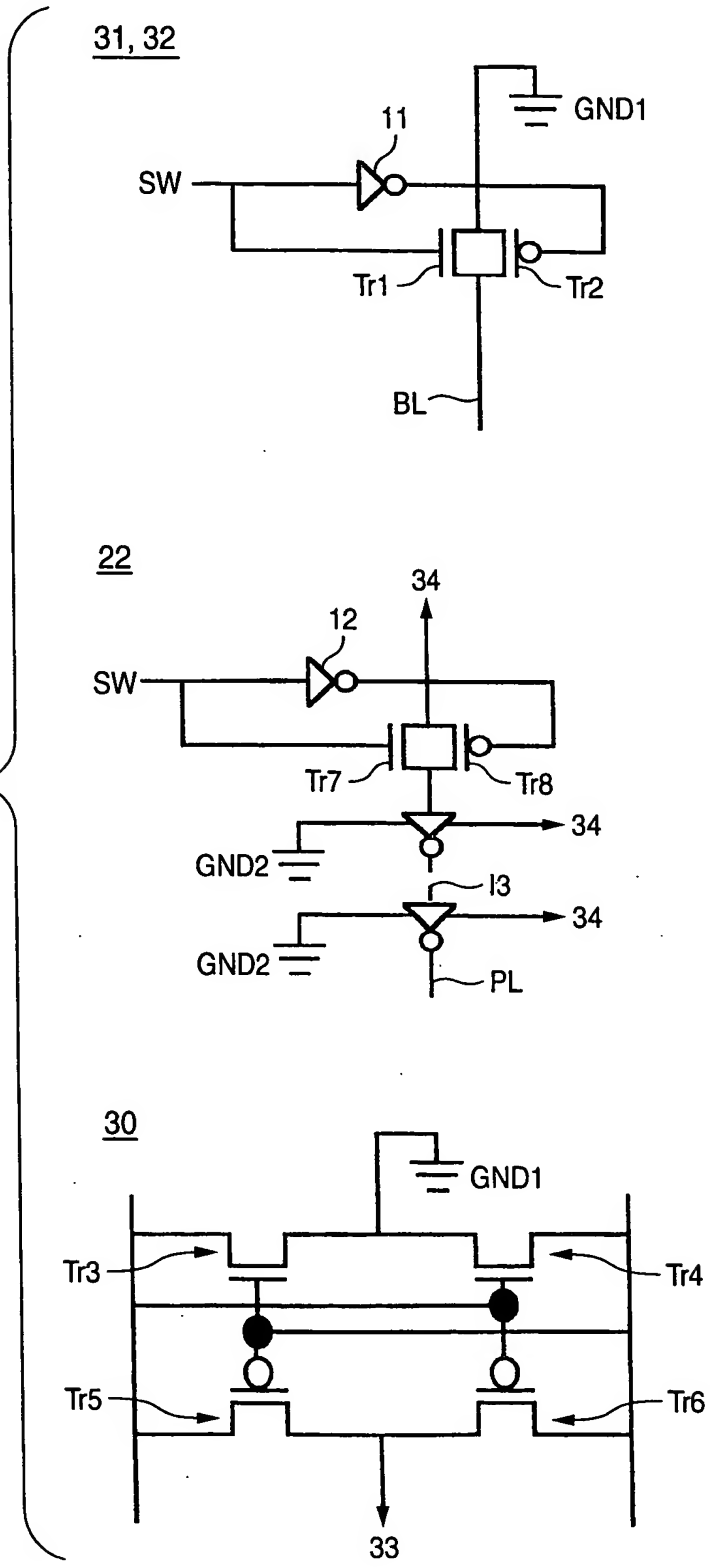

31, 32
GND1
11
SW
Tr1
Tr2
BL
22
34
12
SW
Tr7
Tr8
34
GND2
I3
34
GND2
PL
30
GND1
Tr3
Tr4
Tr5
Tr6
33

FIG. 3A

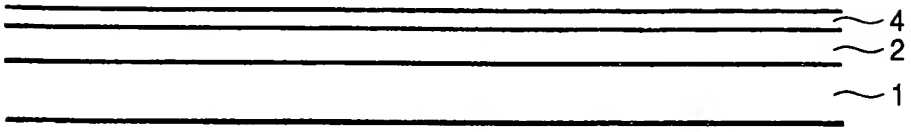


FIG. 3B

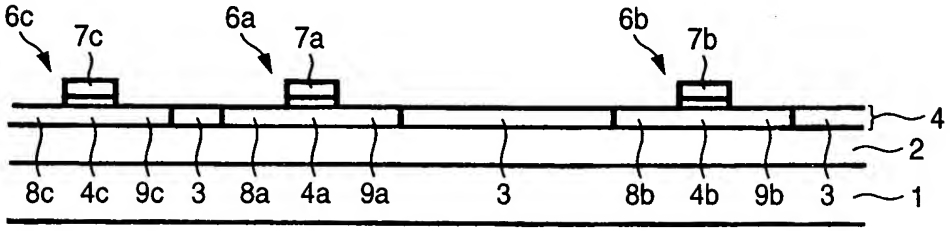


FIG. 3C

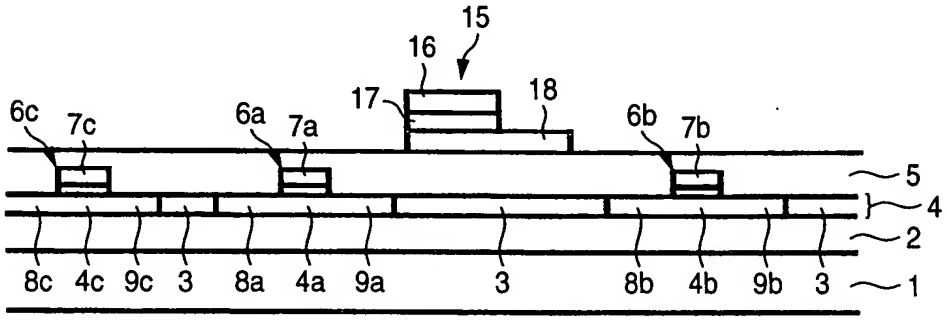


FIG. 3D

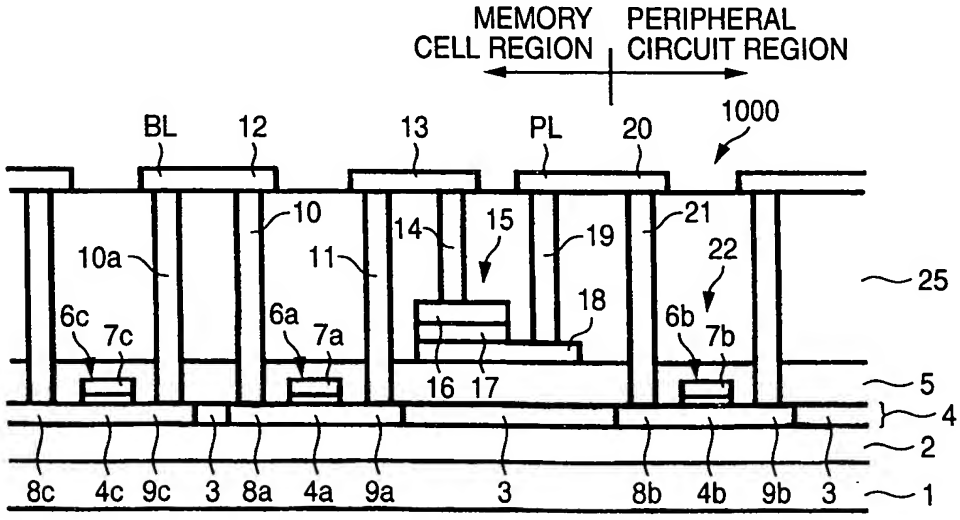
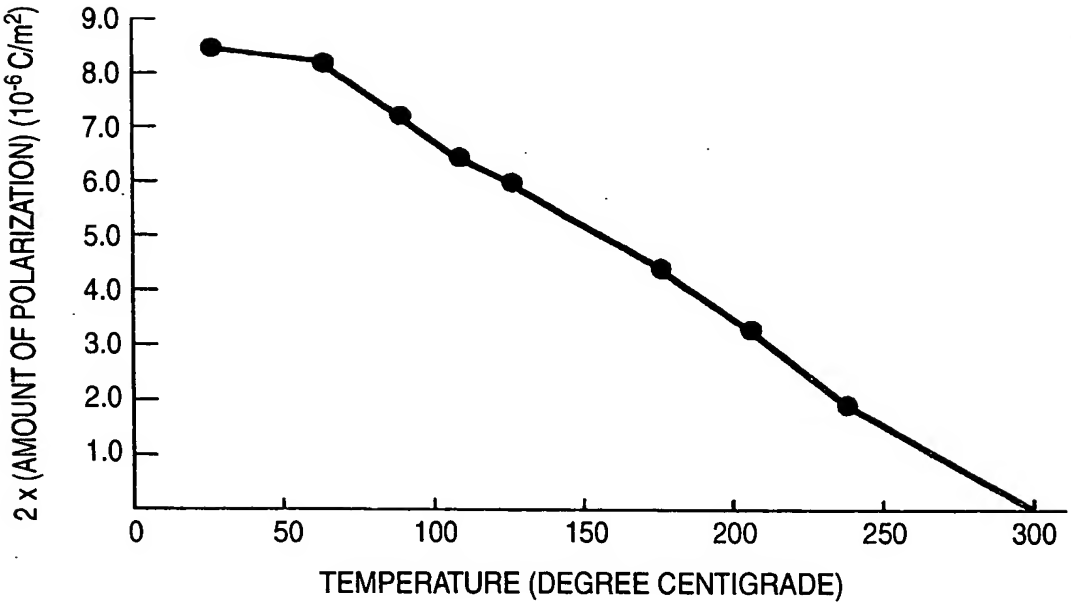


FIG. 4


2 x (AMOUNT OF POLARIZATION) (10^{-6} C/m^2)
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0
50
100
150
200
250
300
TEMPERATURE (DEGREE CENTIGRADE)

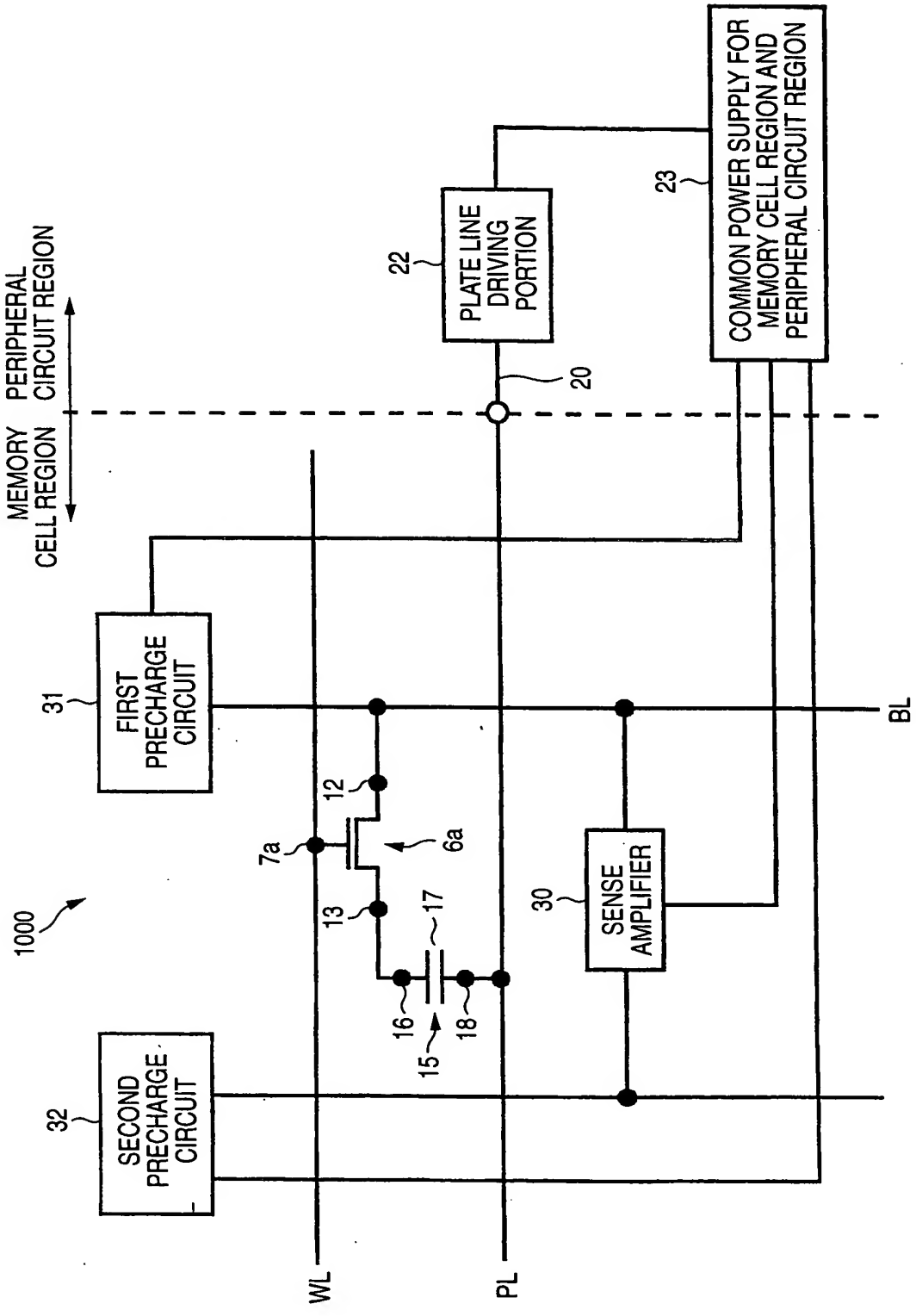

PERIPHERAL CIRCUIT REGION
MEMORY CELL REGION
1000
22
PLATE LINE DRIVING PORTION
23
COMMON POWER SUPPLY FOR MEMORY CELL REGION AND PERIPHERAL CIRCUIT REGION
20
31
FIRST PRECHARGE CIRCUIT
32
SECOND PRECHARGE CIRCUIT
30
SENSE AMPLIFIER
12
13
7a
6a
16
15
17
18
BL
WL
PL

FIG. 5

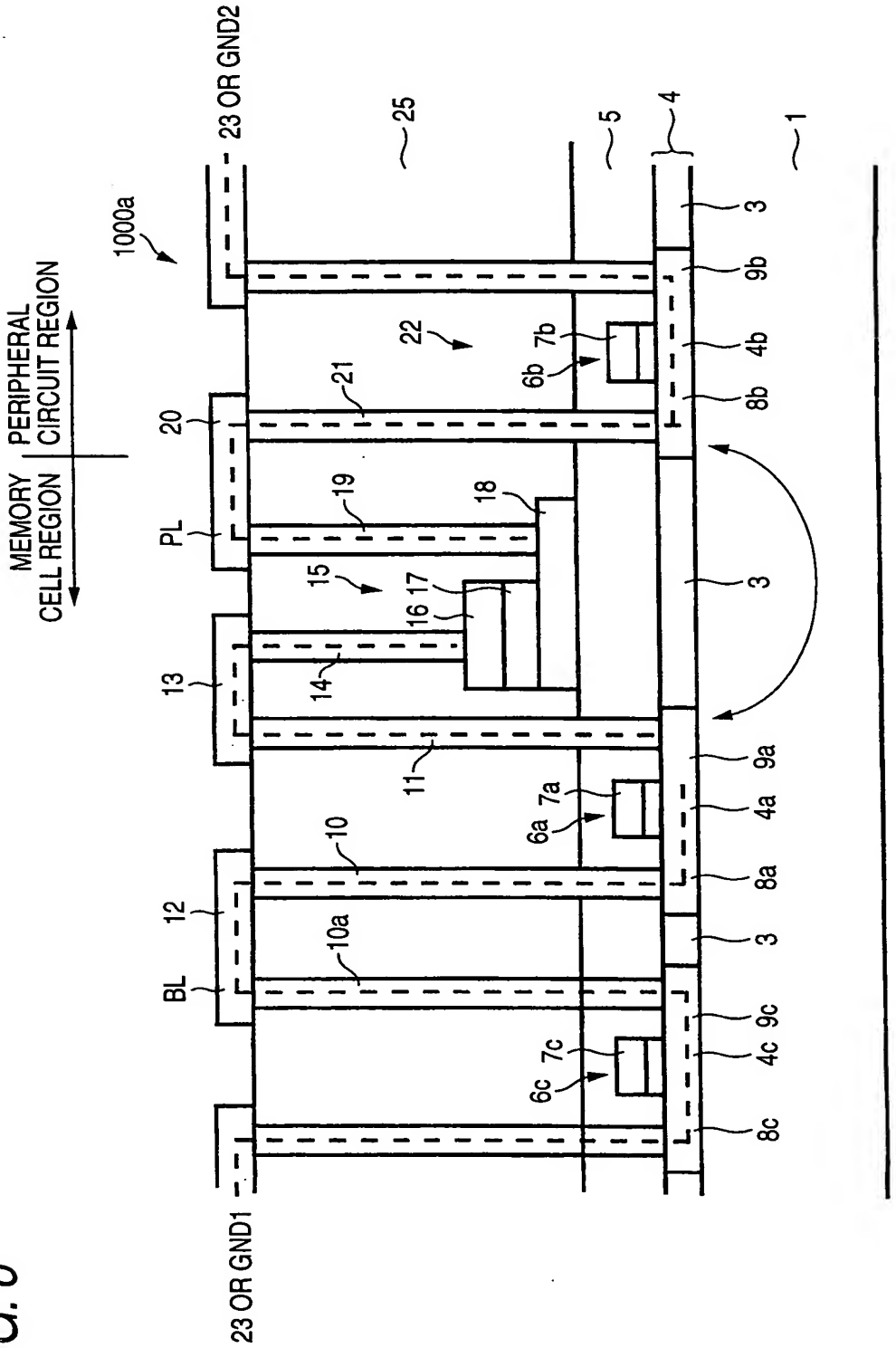

23 OR GND2
25
5
4
1
1000a
PERIPHERAL CIRCUIT REGION
MEMORY CELL REGION
3
9b
4b
8b
22
7b
6b
21
20
PL
19
18
15
16
17
14
13
11
9a
4a
8a
7a
6a
10
12
BL
10a
9c
4c
8c
7c
6c
23 OR GND1

FIG. 6

FIG. 7A

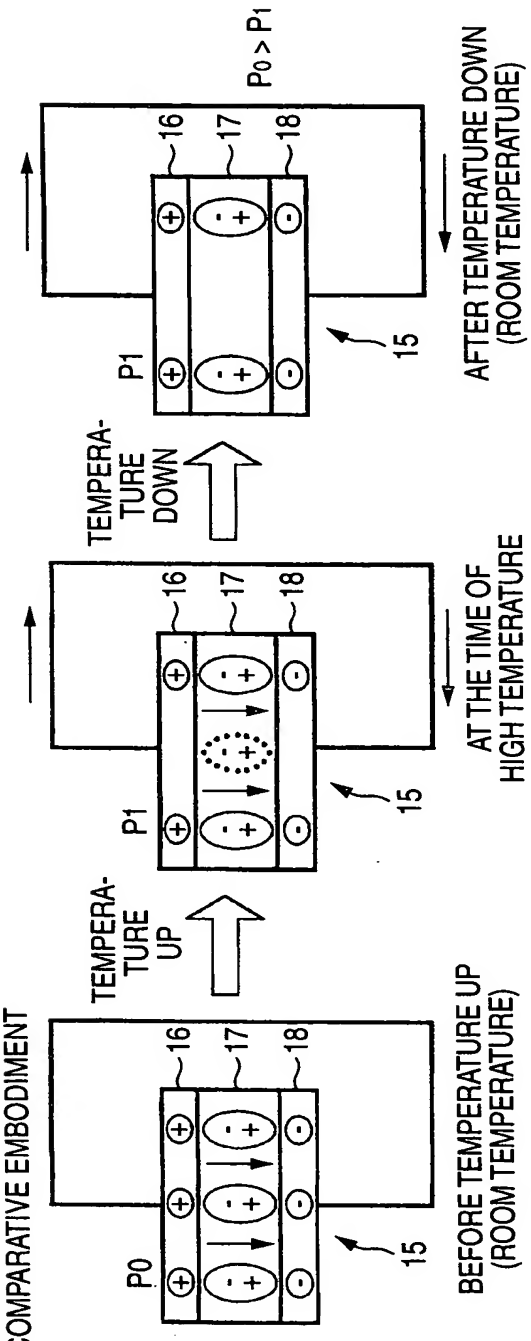

COMPARATIVE EMBODIMENT
BEFORE TEMPERATURE UP (ROOM TEMPERATURE)
TEMPERA-TURE UP
AT THE TIME OF HIGH TEMPERATURE
TEMPERA-TURE DOWN
AFTER TEMPERATURE DOWN (ROOM TEMPERATURE)
P0
P1
P0 > P1
15
16
17
18

FIG. 7B

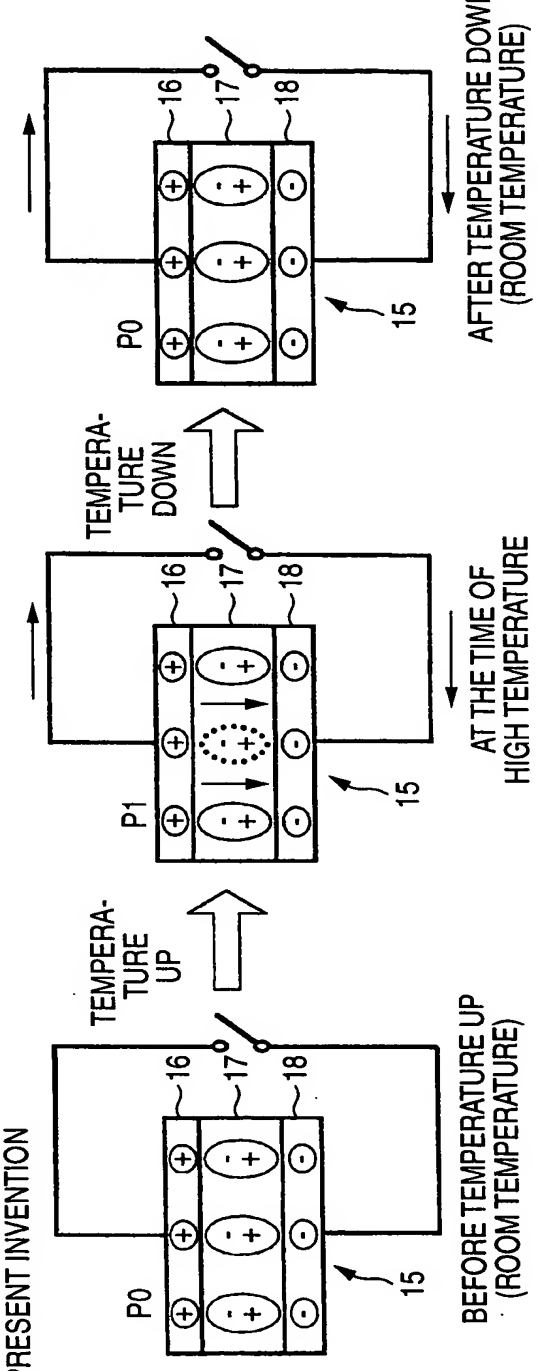

PRESENT INVENTION
BEFORE TEMPERATURE UP (ROOM TEMPERATURE)
TEMPERA-TURE UP
AT THE TIME OF HIGH TEMPERATURE
TEMPERA-TURE DOWN
AFTER TEMPERATURE DOWN (ROOM TEMPERATURE)
P0
P1
15
16
17
18

FIG. 8A

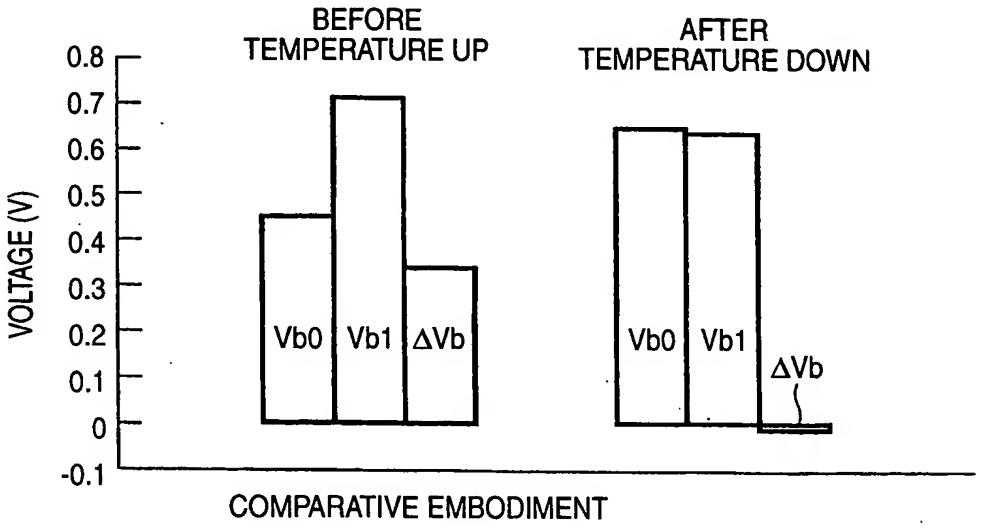

BEFORE
TEMPERATURE UP
AFTER
TEMPERATURE DOWN
VOLTAGE (V)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-0.1
Vb0
Vb1
ΔVb
Vb0
Vb1
ΔVb
COMPARATIVE EMBODIMENT

FIG. 8B

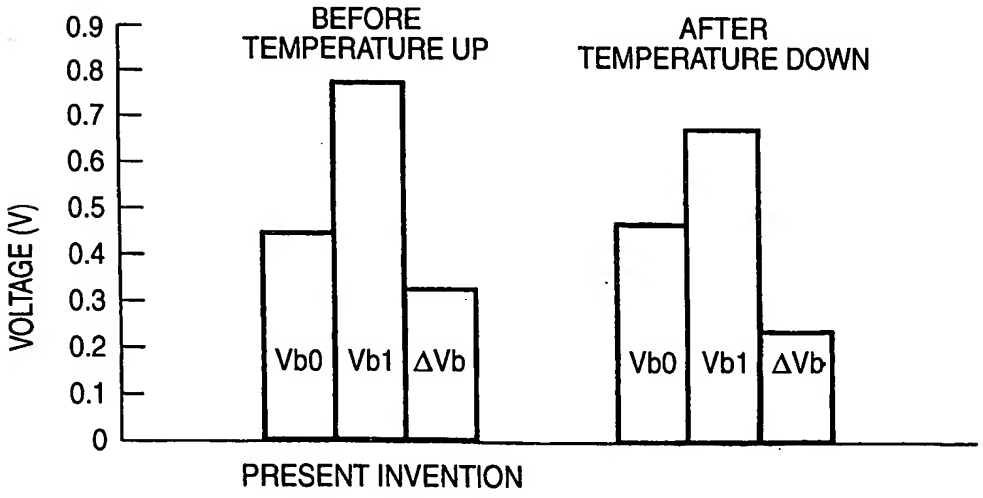

BEFORE
TEMPERATURE UP
AFTER
TEMPERATURE DOWN
VOLTAGE (V)
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Vb0
Vb1
ΔVb
Vb0
Vb1
ΔVb
PRESENT INVENTION

FIG. 9A

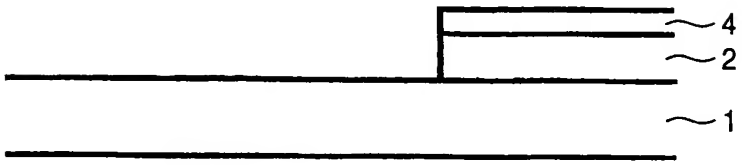


FIG. 9B

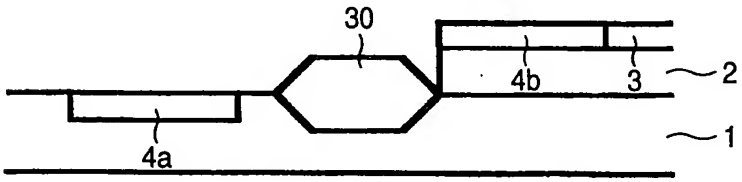


FIG. 9C

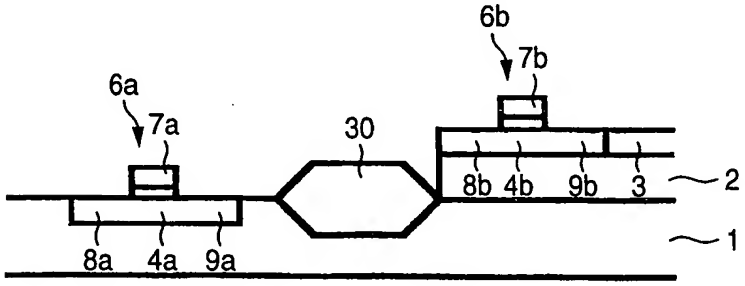
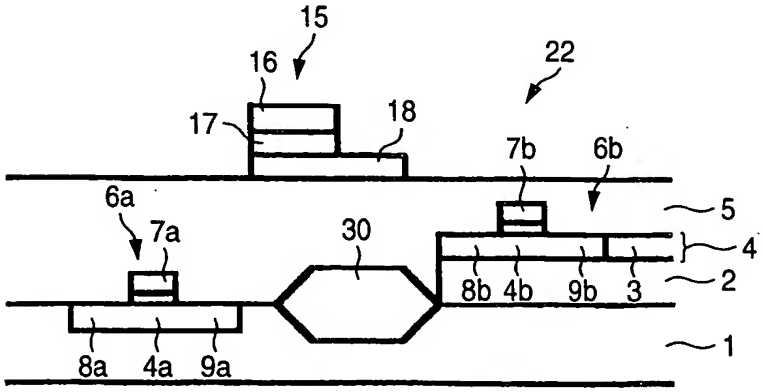


FIG. 9D



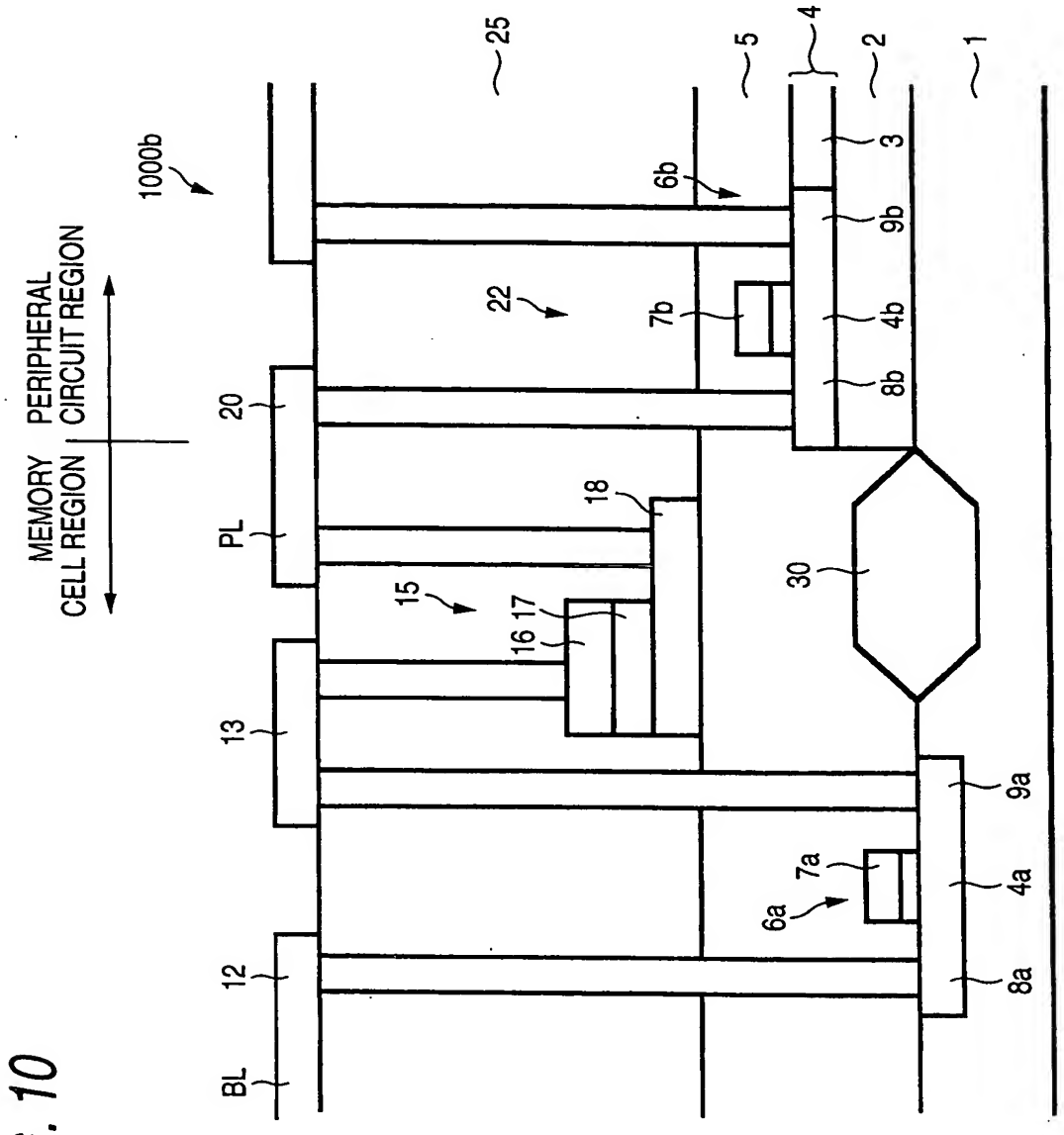

1000b
PERIPHERAL CIRCUIT REGION
MEMORY CELL REGION
25
5
4
2
1
3
6b
9b
22
7b
4b
8b
20
18
PL
30
15
16 17
13
9a
7a
4a
6a
12
8a
BL

FIG. 10

FIG. 11A

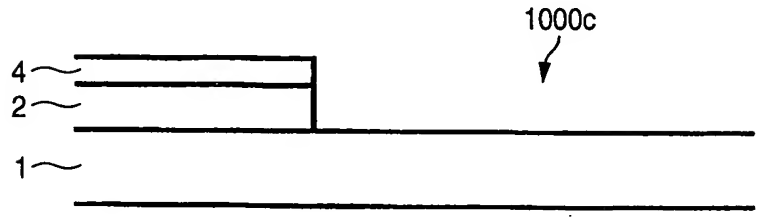


FIG. 11B

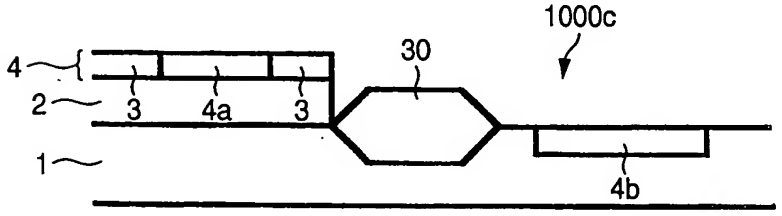


FIG. 11C

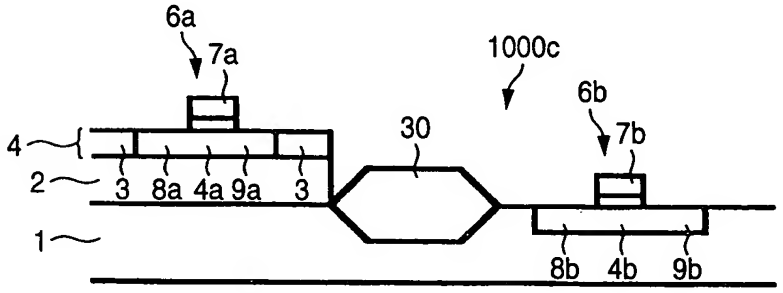
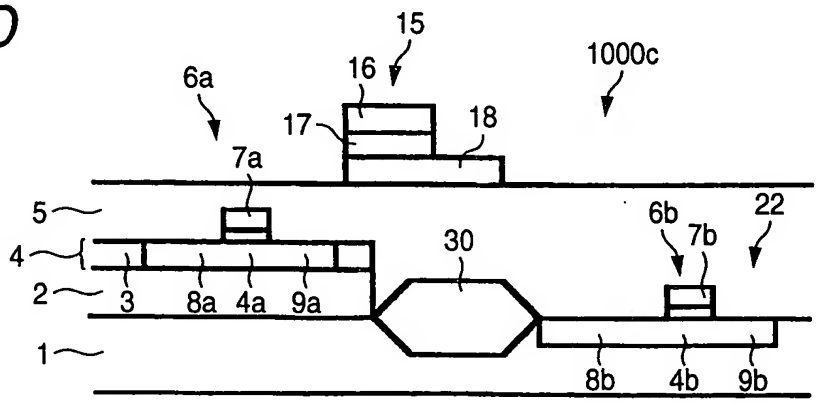


FIG. 11D



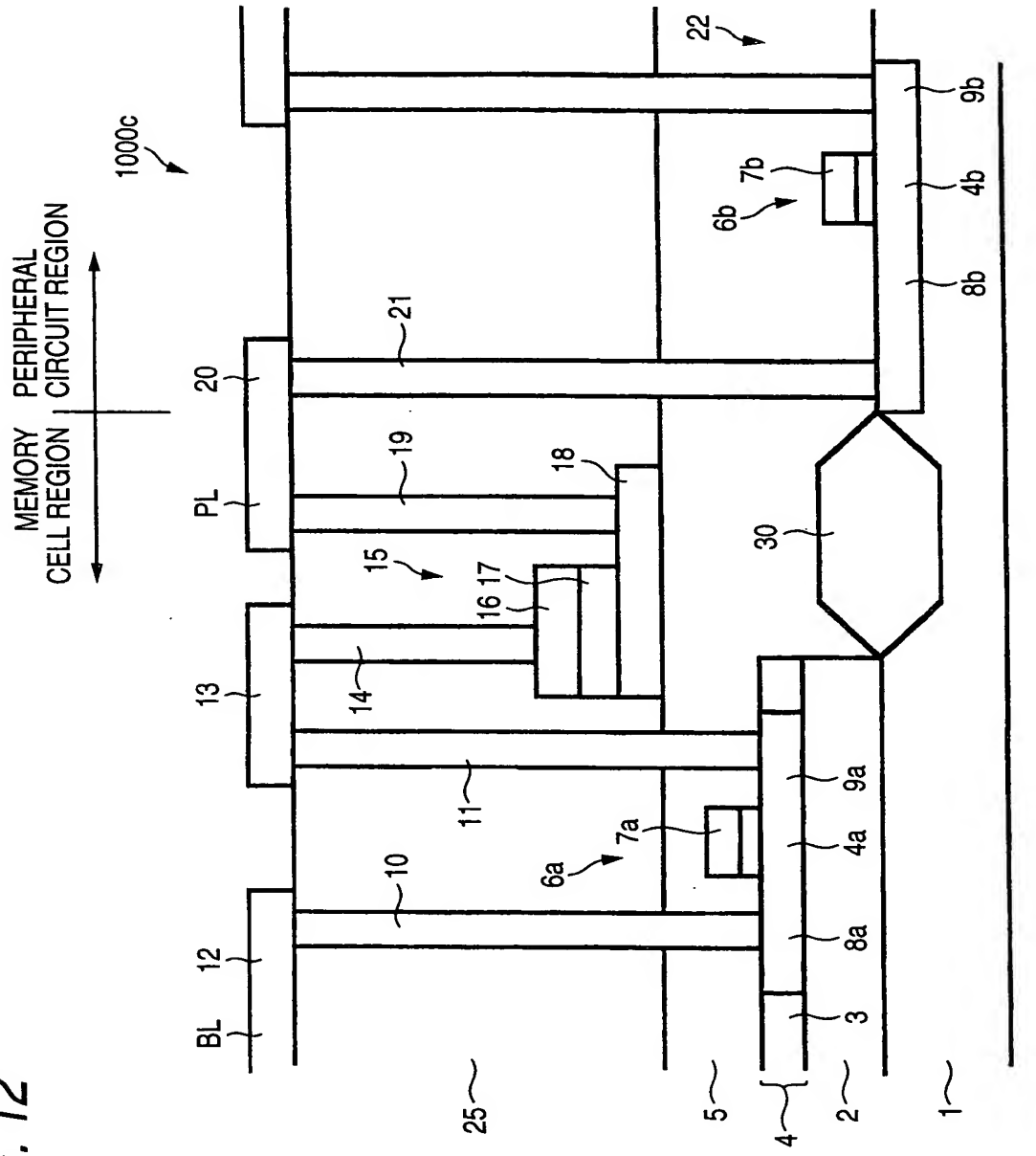

1000c
PERIPHERAL CIRCUIT REGION
MEMORY CELL REGION
BL
12
PL
20
13
10
11
14
15
16
17
18
19
21
22
6a
7a
6b
7b
9a
4a
8a
3
9b
4b
8b
30
25
5
4
2
1

FIG. 12

FIG. 13A

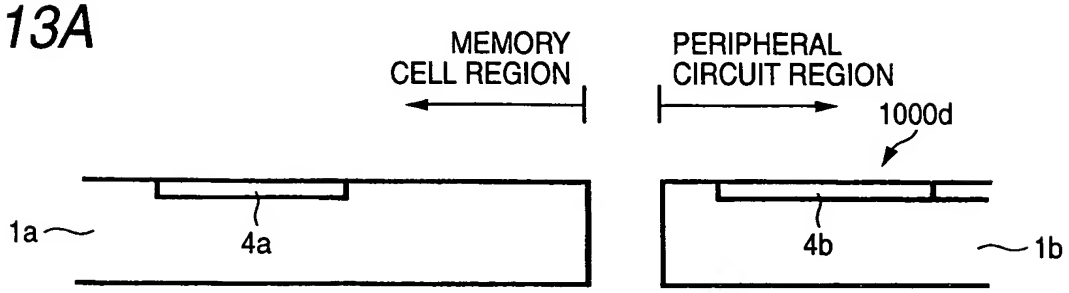


FIG. 13B

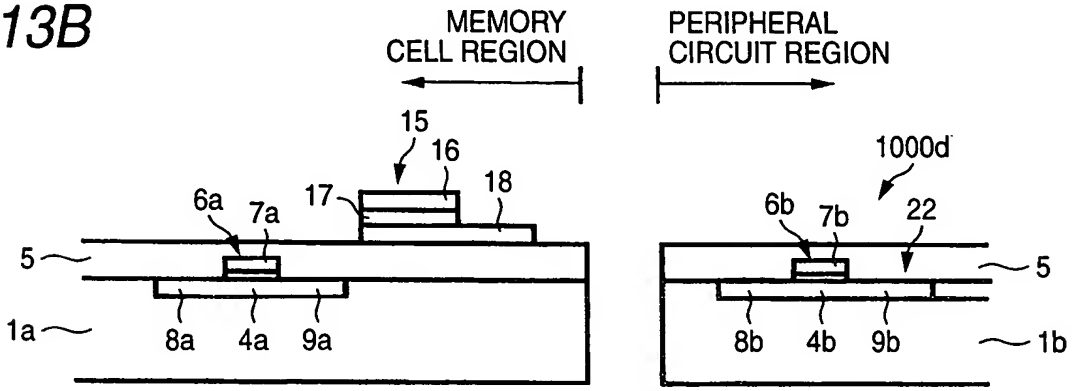


FIG. 13C